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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/691,083	10/18/2000	Milton J. Boden JR.	IR1444 Div. (2-2480)	7041

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 03/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No. 09/691,083	Applicant(s) BODEN ET AL.
	Examiner Brook Kebede	Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,9 and 11-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9 and 11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 20, 2003 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant are advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 3-7, 9, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (US/5,248,627) in view of Kalnitsky (US/5,418,174), and further in view of Wolf et al. (Silicon Processing for the VLSI Era, Process Integration, Volume 2, PP. 194-196, 1990).

Re claims 1 and 9, Williams discloses a MOS gated device which is resistant to single event radiation failure and having improved total dose radiation resistance; said device comprising: a P-type substrate (10 20) having substantially flat, parallel upper (20) and lower (10) surfaces; a plurality of laterally spaced N-type body regions (82 40) extending from said upper surface into said substrate (20); at least one respective P-type source region (84) formed in each of said body regions (82) in said upper surface of said substrate (20) and defining a respective channel region (40) in said upper surface in said body region ; a gate electrode (60) comprised p-type silicon including boron dopants (see Col. 2, lines 51-60) disposed atop and insulated from said channel region and operable to invert said channel region in response to the application of a suitable gate voltage to said gate electrode (60) said gate (60) being insulated form said cannel region (62) by a gate oxide layer (50) comprising silicon dioxide having a thickness of between 500 to1000 angstroms; and a source electrode (84) disposed atop said first surface (20) and connected to each of said source regions (82); said gate electrode being comprised of P-type polysilicon; and an interlayer dielectric layer (6) formed atop gate electrode (60) and having openings (see Fig. 1) therein which said source drain regions (see Figs. 1-7 and also Col. 2, lines 52-68 through Col. 3, lines 1-7).

However, Williams does not specifically disclose the gate oxide layer being radiation hardened.

Kalnitsky discloses semiconductor device that has a gate (16) being insulated form said a cannel region by a gate dioxide layer (14) and said gate dioxide layer being radiation hardened (see Fig. 1 and Col. 1, lines 11-35). Kalnitsky discloses that "Ionizing radiation is known to produce defects in semiconductors. For example, radiation generates unwanted holes and

electrons in gate oxides and other oxide dielectric layers. Throughout the dielectric, radiation generates electron-hole pairs. Some of these electron-hole pairs will recombine while others will not, yielding free electrons and holes. If an irradiated dielectric is a gate oxide, by applying a negative voltage to the gate electrode, the electrons will move toward the substrate and the holes will move toward the gate electrode. If a positive voltage is applied to the gate electrode, the reverse will occur, the electrons will move toward the gate electrode and the holes will move toward the substrate. This movement of and subsequent trapping of electrons and holes on intrinsic trapping sites causes a shift in the threshold voltage due to the radiation. Radiation ultimately induces a build up of positive charge within the dielectric due to large capture cross-sections of hole traps. Various methods have been employed to form radiation hard gate oxides to compensate for the build up of positive charges and to prevent such shifts in the threshold voltage from occurring when the integrated circuit or device is subjected to radiation." (see Kalnitsky Col. 1, lines 10-35).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Williams reference with radiation hardened gate oxide layer as taught by Kalnitsky because the process would have induced a build up of positive charge within the dielectric (i.e. gate oxide) due to large capture cross-sections of hole traps the radiation hardened gate oxide layer and as result shifts in the threshold voltage would have been prevented from occurring when the integrated circuit or device is subjected to radiation.

Although it is well-known in the art to provide doped oxide interlayer dielectric layer which deposited at low temperature such as BPSG, both Williams and Kalnitsky do not specifically disclose the low temperature doped oxide interlayer dielectric layer.

Wolf et al. disclose the use of silane based phosphorus-doped silicon oxide film which deposited at low temperature, a temperature between 350 – 450 °C, (i.e., doped LTO) that have been utilized ILD (interlayer dielectric). As Wolf et al. disclosed, the addition of phosphorous (i.e., dopant) to the film allows reflow to be performed at 1000 °C. Wolf et al. also disclosed silane-based BPSG and boron/phosphorous-doped TEOS also can be reflow at a temperature 850 °C or less and the film would have exhibited low stress and the tendency to crack in the film would have been avoided (see Wolf et al. Page 195-196).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Williams reference with radiation hardened gate oxide layer as taught by Kalnitsky and low temperature doped oxide interlayer dielectric layer as thought by Wolf et al. because the process would have induced a build up of positive charge within the dielectric (i.e. gate oxide) due to large capture cross-sections of hole traps the radiation hardened gate oxide layer and as result shifts in the threshold voltage would have been prevented from occurring when the integrated circuit or device is subjected to radiation and the addition of dopant in low temperature oxide ILD would have been allowed the film or layer to reflow and 1000 °C in case of phosphorous-doped SiO_2 or to reflow below 850 °C in case of silane-based BPSG and boron/phosphorous-doped TEOS and the film would have exhibited low stress and the tendency to crack in the film would have been avoided

Re claim 3, as applied to claim 2 above, Williams and Kalnitsky in combination disclose all the claimed limitations including the limitation wherein said gate dielectric has a thickness of between 500 to 1000 angstroms (see Col. 4, lines 38-43).

Re claim 4, as applied to claim 1 above, Williams, Kalnitsky and Wolf et al. in combination disclose all the claimed limitations including the limitation wherein each of said N-type channel regions has a doping concentration corresponding to that of an approximately 100 KeV phosphorus implant at a dose of about 5.5E13 atoms/cm^{-2} (see Col. 4, lines 15-29).

Re claim 5, as applied to claim 1 above, Williams, Kalnitsky and Wolf et al. in combination disclose all the claimed limitations including the limitation wherein each of said N-type channel regions has a doping concentration corresponding to that of an approximately 100 KeV phosphorus implant at a dose of about 8.0 E13 atoms/cm^{-2} (see Col. 4, lines 15-29).

Re claim 6, as applied to claim 1 above, Williams, Kalnitsky and Wolf et al. in combination disclose all the claimed limitations including the limitation wherein said substrate (10 20) includes a chip of monocrystalline silicon at said lower surface of said substrate and an epitaxial layer formed atop said chip and that is less heavily doped than said chip (see Figs. 6 and 7).

Re claim 7, as applied to claim 1 above, Williams, Kalnitsky and Wolf et al. in combination disclose all the claimed limitations including the limitation wherein said base region includes a portion adjacent to said upper surface that is more heavily doped than another portion of said base region that is adjacent to a lower boundary between said base region and said substrate (see Figs. 6 and 7).

Re claim 11, as applied to claim 1 above, Williams, Kalnitsky and Wolf et al. in combination disclose all the claimed limitations including the limitation a passivation layer formed atop said source electrode (see Figs. 6 and 7).

Re claim 12, as applied to claim 1 above, Williams, Kalnitsky and Wolf et al. in combination disclose all the claimed limitations including the limitation wherein said passivation layer is comprised of low temperature oxide (see Figs. 6 and 7).

Re claim 13, as applied to claim 1 above, Williams, Kalnitsky and Wolf et al. in combination disclose all the claimed limitations including the limitation wherein said gate electrode has a doping concentration corresponding to that of an approximately 50 KeV boron implant of about 5E15 atoms/cm^{-2} (see Figs. 6 and 7).

Response to Arguments

Response to Arguments

4. Applicant's arguments with respect to claims 1, 3-7, and 11-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

THIS ACTION IS MADE NON-FINAL.

Correspondent

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
bk
March 7, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800